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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,513	10/26/2001	Klaus-Peter Behrens	20 01 0631	6890

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EXAMINER	
TORRES, JUAN A	
ART UNIT	**PAPER NUMBER**
2611	

DATE MAILED: 05/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,513	BEHRENS ET AL.	
	Examiner	Art Unit	
	Juan A. Torres	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farwell (US 6324664 B1) and further in view of Alston (US 6055285).

As per clam 1 Farwell discloses a testing unit for testing a device under test (DUT) comprising a signal generator that applies a stimulus signal to the DUT (figure 1 blocks 29 and 33 External test equipment and test bus controller column 4 lines 1-8) and a receiving unit that receives a response signal from the DUT on the applied stimulus signal (figure 1 blocks 29 and 33 External test equipment and test bus controller column 4 lines 1-8); and a synchronizing unit that synchronizes a data flow of the response signal between the DUT and the receiving unit, the synchronizing unit receives a first clock signal from the DUT and a second clock signal of the testing unit (figure 1 blocks 25 and 19, column 3 line 49 to column 4 line 23); the synchronizing unit includes a buffer for buffering data (figure 1 block 25, column 3 line 49 to column 4 line 23); a write unit for writing data from the DUT into the buffer (figure 1 block 19, column 3

line 49 to column 4 line 23); and a read unit for reading out data from the buffer to be provided to the receiving unit (figure 1 block 19, column 3 line 49 to column 4 line 23) . Farwell doesn't specifically disclose that the first clock signal controls a write access onto the buffer; and that the second control signal controls a read access onto the buffer. Alston discloses a synchronizing unit for synchronizing a data flow of the response signal between two clock domains (figure 2 column 8 line 57 to column 9 line 12) where the first clock signal controls a write access onto the buffer (figure 2 blocks 140 column 8 lines 57-62); and that the second control signal controls a read access onto the buffer (figure 2 blocks 142 column 8 line 60 to column 9 line 3). Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been synchronizing the transfer of data from a transmitting circuit operating in a first clock domain to a receiving circuit operating in a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

As per claim 2 Farwell and Alston disclose claim 1. Alston also discloses that the buffer comprises a register structure with a plurality of registers (figure 3 blocks 300, 304 and 306 column 9 line 49-50). Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in

the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been synchronizing the transfer of data from a transmitting circuit operating in a first clock domain to a receiving circuit operating in a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

As per claim 3 Farwell and Alston disclose claim 2. Alston also discloses a write pointer that moves between the pluralities of registers for defining one of the plurality of registers to receive and buffer from one clock domain (figure 2 block 214 column 8 lines 62-66), and a read pointer that moves between the plurality of registers for defining one of the pluralities of registers to be read out (figure 2 block 216 column 9 lines 4-12). Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been synchronizing the transfer of data from a transmitting circuit operating in a first clock domain to a receiving circuit operating in a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

As per claim 4 Farwell and Alston disclose claim 3. Alston also discloses that the write pointer is clocked by the first clock signal for successively writing successive data words from one clock domain to different registers (figure 3 block 122 and 106 column 9

lines 34-38), and the read pointer is clocked by the second clock signal for successively reading out successive data words buffered in the plurality of registers (figure 5 block 132 and 108 column 17 lines 18-21). Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been synchronizing the transfer of data from a transmitting circuit operating in a first clock domain to a receiving circuit operating in a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

As per claim 5 Farwell and Alston disclose claim 1. Alston also discloses that the write unit comprises a latch controlled by the first clock signal, so that successive data words can be latched with the first clock signal and thus successively written into the buffer (figure 3 block 300 column 9 lines 34-40). Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been synchronizing the transfer of data from a transmitting circuit operating in a first clock domain to a receiving circuit operating in a second clock domain, where

the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

As per claim 6 Farwell and Alston disclose claim 1. Alston also discloses that the buffer provides an initial delay time between a first valid write access and a first valid read access (figure 6 block 310 flip-flops 330-332-334-336 column 17 lines 23-28). Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been synchronizing the transfer of data from a transmitting circuit operating in a first clock domain to a receiving circuit operating in a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

As per claim 7 Farwell and Alston disclose claim 6. Alston also discloses that the initial delay time is dependent on the maximum expected variation between such write and read accesses (figure 3 block 310 flip-flops 330-332-334-336 column 7 lines 23-28). Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been synchronizing the transfer of data from a transmitting circuit operating in a first clock domain to a receiving

circuit operating in a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

As per clam 8 Farwell discloses a testing method for testing a device under test (DUT), the method comprising the steps of applying a stimulus signal to the DUT, where the DUT outputs data in response to the stimulus signal (figure 1 blocks 29 and 33 External test equipment and test bus controller column 4 lines 1-8); writing the data into a buffer, where a first clock signal is provided by the DUT (figure 1 blocks 19 and 25, column 3 line 49 to column 4 line 23); and reading the data from the buffer where a second clock provided by the receiving unit (figure 1 blocks 19 and 25, column 3 line 49 to column 4 line 23); and communicating the data from the buffer to the receiving unit (figure 1 blocks 19, 29 and 33, column 3 line 49 to column 4 line 23). Farwell doesn't specifically disclose that the writing employs the first clock signal that controls a write access to the buffer; and that the reading employs a second clock signal that controls a read access of the buffer. Alston discloses that the writing employs the first clock signal that controls a write access to the buffer (figure 2 blocks 140 column 8 lines 57-62); and that the reading employs a second clock signal that controls a read access of the buffer (figure 2 blocks 142 column 8 line 60 to column 9 line 3). Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been synchronizing the transfer of data

from a transmitting circuit operating in a first clock domain to a receiving circuit operating in a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

As per claim 9 Farwell and Alston disclose claim 8. Alston also discloses initializing a first valid write access and/or a first valid read access (figure 6 block 310 flip-flops 330-332-334-336 column 17 lines 23-28). Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been synchronizing the transfer of data from a transmitting circuit operating in a first clock domain to a receiving circuit operating in a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Juan Alberto Torres
5-4-2006